Large-area formation of self-aligned crystalline domains of organic semiconductors on transistor channels using CONNECT

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The electronic properties of solution-processable small-molecule organic semiconductors (OSCs) have rapidly improved in recent years, rendering them highly promising for various low-cost large-area electronic applications. However, practical applications of organic electronics require patterned and precisely registered OSC films within the transistor channel region with uniform electrical properties over a large area, a task that remains a significant challenge. Here, we present a technique termed "controlled OSC nucleation and extension for circuits" (CONNECT), which uses differential surface energy and solution shearing to simultaneously generate patterned and precisely registered OSC thin films within the channel region and with aligned crystalline domains, resulting in low device-to-device variability. We have fabricated transistor density as high as 840 dpi, with a yield of 99%. We have successfully built various logic gates and a 2-bit half-adder circuit, demonstrating the practical applicability of our technique for large-scale circuit fabrication.

organic semiconductors | patterning | small molecules | transistors | circuits

Organic electronics are being rapidly developed to pave the way for low-cost, large-area, flexible, and transparent electronics, such as active matrix displays, radiofrequency identification tags, and integrated logic circuits (1–6). Solution-processable small-molecular organic semiconductors (OSCs) are promising for these applications because of their high performance in organic thin-film transistors (OTFTs) and their low-cost, large-area processability (7–11). Recently, solution-processed small-molecule OSCs have shown record-breaking charge carrier mobility in thin-film transistors, furthermore providing the exciting prospect of organic electronics (9–12). However, significant challenges still remain to realize practical applications of organic electronics. First, patterning and precisely registering OSCs within the channel region is imperative to reduce leakage current between neighboring TFTs and parasitic capacitance, and to increase device yield. Second, low variability in electrical characteristics is essential so that all OTFTs work in concert with one another to carry out proper device functionalities. Last, all these features must be achieved in a scalable and economical manner, as large area and low cost are key advantages for organic electronics.

To address the above challenges, various groups have developed methods to pattern OSCs (3, 9, 13–24), such as templating OSCs (14, 19–21), inkjet printing (9, 18), gravure printing, and other roll-to-roll coating methods (25–27). In addition, the use of solvent wetting/dewetting surface treatments has been widely used in conjunction with the patterning methods described above (10, 11, 13, 15–17, 22, 28, 29). Despite some promising results, there remain shortcomings that potentially limit their practical applicability. Primarily, it is difficult to align drain and source electrodes to OSCs, as standard photolithography generally cannot be directly applied due to solvent-induced degradation. Additive printing methods to place OSCs on electrodes or vice versa is often difficult to achieve, especially as the density of TFTs become higher (30). For instance, alignment using inkjet printing is restricted by the registration capability of the instrument, whereas the size of each OTFT is limited by the droplet size attainable (22, 31). Another potential issue with these methods is the variance in electrical characteristics of TFTs due to the difficulty in obtaining uniform crystal growth on isolated TFTs over large areas (9, 15, 21, 27, 28, 31–35). Even single crystalline domains of patterned TFTs may have large variability in electrical characteristics as a result of random orientation and size variance.

Self-alignment of OSCs on electrodes has been developed by various groups to overcome misalignment (36, 37). Vertical TFTs were created to achieve self-aligned small channels (36, 37); however, achieving high-device performance requires precise control of device fabrication. UV light exposure after electrode patterning can be used to generate a hydrophilic channel between the electrodes, where OSCs can be selectively isolated and deposited (38–40). However, this method is limited to transparent substrates and only short channels (<500 nm). The UV light can

Significance

Solution-processed organic electronics are expected to pave the way for low-cost large-area electronics with new and exciting applications. However, realizing solution-processed organic electronics requires densely packed transistors with patterned and precisely registered organic semiconductors (OSCs) within the transistor channel with uniform electrical properties over a large area, a task that remains a significant challenge. To address such a challenge, we have developed an innovative technique that generates self-patterned and self-registered OSC film with low variability in electrical properties over a large area. We have fabricated highest density of transistors with a yield of 99%, along with various logic circuits. This work significantly advances organic electronics field to enable large-scale circuit fabrication in a facile and economical manner.

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also damage the OSC–dielectric interface, creating traps that increase the variability between TFTs. Contact directed nucleation have previously been used to increase crystallinity in the channel region (41). However, grain boundaries remain and result in large variance in OTFT performance. Mannsfeld et al. (42) have reported solution deposition of OSC crystals on electrodes using a liquid vortex method, but the OSC crystals have incomplete channel coverage, leading to varying electrical characteristics. Polycrystalline thin films of pentacene have been formed in between electrodes using vapor deposition, but patterning is required to isolate the area of deposition (43).

In this study, we introduce a highly effective method—controlled OSC nucleation and extension for circuits (CONNECT)—that uses differential surface wetting properties combined with solution shearing (44, 45) to pattern and align crystalline domains of OSCs selectively between source and drain electrodes in a single step. This method of patterning overcomes a number of challenges previously encountered with other patterning methods described above. First, as the electrodes themselves serve as templates for patterning OSCs, extra steps to pattern and register OSCs to the channel region are not necessary. Second, this method ensures that each bridging event yields aligned crystalline domains from a single nucleation site across the channel, which results in OTFTs with relatively low variance in electrical characteristics. Our method was observed to work over a wide range of channel lengths, ranging from 0.5 to 20 μm, both with photolithographically patterned and inkjet-printed electrodes, making our process versatile to different electrode types and a wide range of OTFT densities. We have attained OTFT densities as high as 840 dpi, which is among the highest achieved in OTFTs (46). Last, our method was shown to be scalable to a large area and had a high crystal CONNECT yield of 99%. As a first demonstration of the potential of our method, we have fabricated various logic gates and a 2-bit half-adder circuit consisting of 60 source/drain channel regions. Together, these demonstrations render our method highly promising for various organic electronic applications where ease of processability, scalability, flexibility in OTFT density, device-to-device uniformity, and yield are of great importance.

Results

Patterning OSCs by CONNECT. Photolithography was first used to fabricate bottom-contact Au electrodes (2-nm Cr and 40-nm Au). We then used the selective surface reactivity of SiO_2 and Au to silane and thiol, respectively, to functionalize each surface with different self-assembled monolayers (SAMs). SiO_2 was first modified with an *n*-octadecyltrichlorosilane (OTS) SAM, rendering it lyophobic. The OTS physisorbed on the Au surface was easily removed by heating the substrate to 120 °C for 10 min. Thereafter, the substrate was modified with a thiophenol SAM, which increased the wetting of electrodes to solution. Due to the wetting and dewetting properties of the Au electrode and SiO_2, respectively, the subsequent solution-sheared 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) deposition occurred selectively on the electrodes and the channel region, whereas the rest of the substrate had no TIPS-pentacene deposited (Fig. 1*A*). As a control experiment, we have sheared over a substrate without any SAM treatment and have observed no patterning of TIPS-pentacene (Fig. S1*A*).

CONNECT works by limiting OSC nucleation and promoting crystal growth in selected areas during solution shearing. Fig. 1*B* is a schematic diagram of one of our electrode sets, and Fig. 1*C* depicts the nucleation and crystal growth process. As shearing begins at the top, multiple nucleation and crystallization events occur in the nucleation region. The selection and growth region that follows the nucleation region selects a crystalline domain to propagate downward (Fig. S1 *B* and *C*). When the evaporation front reaches the trailing electrode, the liquid bridges both the leading electrode and the trailing electrode. Previously, we have shown that crystal growth begins from the air–solvent interface and proceeds toward the substrate during solution shearing (47). In this work, we match the timescale of vertical crystal growth with the lateral crystal growth, to ensure that the crystalline domain that was growing on the leading electrode will extend to the trailing electrode and cover the OTFT channel before the solution dries (see *SI Note 1* for a detailed description of this phenomenon). This method ensures that each bridging event results in aligned crystalline domains, as we have previously shown that the fast growth axis of the OSC crystal aligns itself with the direction of solution shearing, i.e., perpendicular to the channel length in this case (45). To show the applicability of our technique to another molecule, we have also successfully demonstrated CONNECT with fluorinated 5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES-ADT) (see Fig. S2 for optical images and electrical data). We expect CONNECT to be generally applicable to a wide range of other OSCs if the OSC nucleation location and crystal growth rate can be controlled, and the OSC can grow crystals large enough to cover the electrode and the channel region. However, we note that, depending on the solvent and OSC used, further exploration and optimization of SAM treatment may be required to ensure surface energies that enables wetting and dewetting in the desired regions.

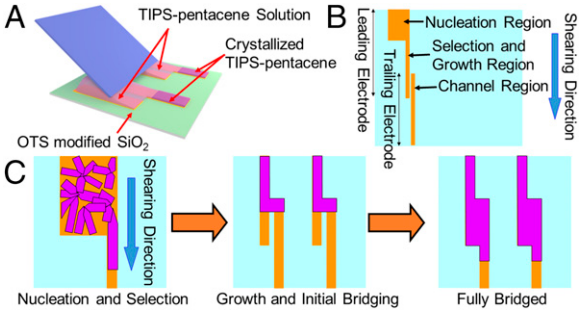

Fig. 1. Schematic process of CONNECT. (*A*) Schematic depiction of film growth during solution shearing. (*B*) Depiction of our electrode design with labeling of different regions. (*C*) Description of CONNECT: controlled nucleation occurs in the nucleation region followed by selection and growth of a crystalline domain down the electrode toward the channel region. Film growth from the air–solution interface to the solution–substrate interface during solution shearing allows channel bridging by crystals.

Characterization of Patterned TIPS-Pentacene Domains. Fig. 2*A* is an optical image of electrodes patterned on a 4-in wafer with TIPS-pentacene deposited over a $2 \times 2\text{-in}^2$ area, showing the scalability of our technique. Fig. 2*B* is a large image of a section on the wafer showing selectively patterned TIPS-pentacene crystals on the electrodes and within the channels. Fig. 2 *C* and *D* are large-area and close-up images of a dense array of electrodes, with a density of 33 OTFTs per millimeter (840 TFTs per inch). Rotation of the sample under cross-polarized light (Fig. 2 *E* and *F*) extinguishes light of all TIPS-pentacene crystals at ±45° due to the twinning behavior of TIPS-pentacene crystals, confirming the well-aligned, fast growth axis of the crystals along the shearing direction (i.e., the growth of either crystal twin is possible, with the fast growth axis as the common boundary) (45). The handedness of the crystal should not impact the charge transport properties of the resulting OTFT. Grazing X-ray diffraction also confirms aligned TIPS-pentacene growth (Fig. S3). With optimized electrode dimensions and shearing conditions, it is perceivable that an even higher density of OTFTs can be achieved using our technique.

Optical and atomic force microscopy (AFM) images show that cracks in the crystal from one electrode extend to the other,

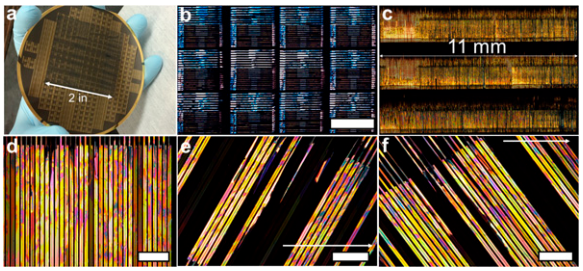

Fig. 2. Optical characterization of patterned TIPS-pentacene crystalline domains. (*A*) Image of TIPS-pentacene sheared on a 4-in wafer over a 2 x 2-in area. (*B*) Cross-polarized optical image of a section of the wafer shown in *A*. The transistors had electrode widths that were 50 or 10 μm and a pitch of 200 or 120 μm. (Scale bar: 3,000 μm.) (*C*) Large-area cross-polarized optical image of dense arrays of electrodes with 33 TFTs per millimeter. (*D*) Close-up image of *C*, showing well-aligned patterned crystals on the electrodes and within the channel regions. (Scale bar: 200 μm.) (*E* and *F*) Rotated images of *D*, showing the extinguishing of light at ±45°. The arrows point to the same electrode. (Scale bar: 200 μm.)

confirming the same crystalline domain extending across the channel (Fig. S4 *A* and *B*). There is also a dip of 41 nm in the AFM image near the electrode edge, suggesting that the film conforms to fill up the channel space between the electrodes (Fig. S4*B*, *Inset*). We have also taken an AFM image of the TIPS-pentacene in contact with the oxide surface, which showed no apparent grain boundaries with roughness less than 1 nm, confirming highly crystalline film growth over the channel region (Fig. S5). Because charge transport occurs near the semiconductor/dielectric interface, it is important that TIPS-pentacene fully contacts the SiO_2 dielectric and the electrodes. A cross-sectional transmission electron microscopy image (Fig. S4*C*) shows intimate contact of TIPS-pentacene to both the SiO_2 surface and the Au electrode.

Electrical Characterization of TFTs. The channel length of our OTFTs was set at 2 μm, whereas the channel width was set at 500 and 1,000 μm. CONNECT was performed on four substrates, each with an area of ~2 × 2 cm^2. The substrates yielded a maximum of one to two TFTs that did not bridge out of ~110 OTFTs—resulting in a yield of >99%. High bridging yield of >99% was also obtained over a larger 2 × 2-in^2 area, although we have found some regions of overgrown crystals due to spatial variability of the solution concentration during solution shearing. Flow enhancement techniques (10) can potentially resolve this issue and is currently being investigated. OTFT yield is sparsely mentioned in literature, but a few examples are available for comparison. Hambsch et al. (27) have shown that gravure printing of polymers can yield 75% working OTFTs. Recently, Arias and coworkers (48) have shown fully solution-deposited OTFTs with a yield of 96%. We characterized 120 randomly selected OTFTs. Fig. S6 contains images of some of the OTFTs measured. Fig. 3*A* is a plot of overlaid transfer curves of 120 TFTs measured at $V_{DS} = -50$ V, whereas the *Inset* is an optical image of some of the measured TFTs. The average mobility of our TFTs were 0.167 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (highest mobility at 0.4 $cm^2/V \cdot s$) with a relative variance (SD divided by average) of 28% over the 120 devices tested (histogram and table in Fig. S7). In comparison, other patterning methods used to create patterned OSCs for isolated OTFTs have shown relative variances ranging from 20% to 84% (9, 15, 17, 22, 31, 32, 35, 42, 48–54). For example, Li et al. (15) have shown that using a PMMA:C8BTBT blend on a solution wetting pattern can deposit crystal plates that have a mobility relative variance of >40%. The relatively low variance in electrical characteristics of our OTFTs can be attributed to both the directly bridging crystalline domains that reduce the number of grain boundaries in the channel region and the aligned domains that reduce the impact of the anisotropic charge transport behavior of TIPS-pentacene. The mobilities measured here are perpendicular to the direction of the fast crystal growth axis, and for TIPS-pentacene, previous literature has shown that this is the slow charge transport direction for single crystalline domains by a factor of 3.5–10 (55, 56). Hence, lower mobility obtained in our OTFTs can be attributed to the slow transport direction across the channel, and we predict that our method will result in larger charge carrier mobilities if the direction of fast charge transport is perpendicular to the direction of fast crystal growth. In addition, the mobility calculated is likely underestimated due to the short-channel length of our device, which results in contact resistance contributing significantly to the total resistance of the device. Fig. 3*B* is a typical output curve of with V_G varying from 30 to −50 V in 16-V steps. The diotic behavior of the output curve indicates dominating contact resistance. The contact resistance can potentially be reduced by techniques like contact doping or using high work function metals.

Fig. 3*C* shows the histogram of on-current density of the 120 OTFTs. Here, we see that on-current density ranged within a factor of 3 and a relative variance of 26%, furthermore indicating relatively uniform crystalline domains of TIPS-pentacene device-to-device. This is especially important for logic circuit application as the relative on-conductance of various OTFTs in a circuit determines the direction of current flow, which enables proper logic functionalities. The average threshold voltage of our OTFTs was −6.77 V (histogram and table in Fig. S7). Typical hysteresis characteristic is depicted in Fig. S8. Fig. 3*D* is a histogram of log of on/off ratios [$\mathrm{Log}(I_{ON}/I_{OFF})$]. Our OTFTs had a variance in $\mathrm{Log}(I_{ON}/I_{OFF})$ of 14.5%, with an average on/off ratio of 6.15 × 10^3. The variation in on/off ratio can be attributed to the variation in the thickness of the TIPS-pentacene film, where the poorly gated TIPS-pentacene layer away from the dielectric/semiconductor interface contributes to the off-current. The thickness of the film can be controlled by finer control of solution shearing parameters, which can potentially increase the overall on/off ratios of the OTFTs.

Electrical Characterization of Organic Circuits. The high uniformity in on-current density and on/off ratios of our TFTs is highly promising for large-scale circuit fabrication. As a proof of concept,

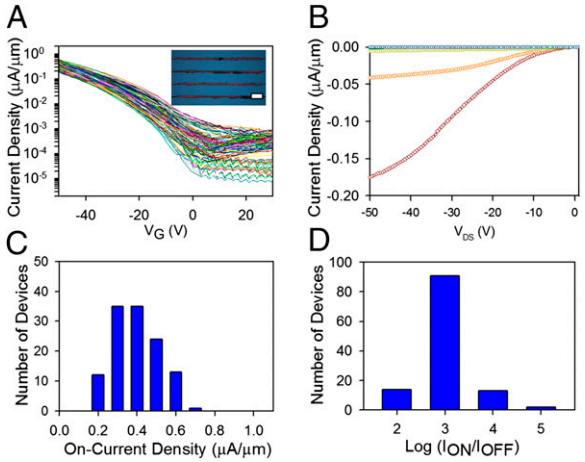

Fig. 3. Electrical characterization of bridged TIPS-pentacene TFTs. (*A*) Overlaid transfer curves of 120 OTFTs at −50 V_{DS}. The *Inset* is an optical image of several bridged OTFTs. (Scale bar: 100 μm.) (*B*) Representative output characteristics of TIPS-pentacene OTFTs. The V_G was swept from 30 to −50 V in 16-V steps. (*C*) Histogram of on-current density of 120 OTFTs. (*D*) Histogram of log of on/off ratio of 120 OTFTs.

we have built various "universal" logic gates and a 2-bit half-adder circuit. Fig. 4*A* is a circuit diagram of a P-type metal–oxide–semiconductor (PMOS) inverter (NOT gate) along with our design layout. To achieve optimal switching, we have designed the resistance of the load transistor to be approximately six times that of the driver transistor by using an array of six shorted electrode pairs as the driver transistor and a single electrode pair as the load transistor. The load transistor was designed to allow voltage (V_{BIAS}) to be applied to the gate electrode to ensure that the load resistor is always on and to adjust its resistance as needed. An array of electrodes was used as the driver transistor to conserve vertical space, as vertical dimensions of each electrode pair were ~45 times that of its lateral dimensions. We have designed our nucleation region with triangles, as previous studies have shown that sharp edges increase the probability of nucleation (10), which induce nucleation and crystallization over a shorter distance. As seen in the polarized optical image in Fig. 4*B* and schematically depicted in Fig. 4*A*, nucleation occurred at the sharp corners of the triangles forming numerous crystal grains. Subsequently, as shearing progressed downward, one crystalline domain selectively propagated down the electrodes and would eventually bridge to form OTFTs (Fig. 4*C*). Fig. 4*D* is a representative voltage transfer curve of our inverter and its corresponding gain versus V_{IN} plot with V_{DD} = 40 V, V_{BIAS} = −20 V, and V_{IN} swept from 0 to 40 V. The voltage transition occurs from 17 to 24 V with a gain of 14.5, yielding noise margin of ~10–13 V. Such characteristics indicated that our inverter can be used to switch logic gates without losing logic integrity.

By placing a second driver transistor in parallel or in series, we have constructed NAND gate (low output only when both inputs are high) and NOR gate (high output only when both inputs are low), respectively (Fig. S9 *A–D*). V_{DD} was set at 40 V, whereas A and B inputs were either 0 or 40 V. We have observed proper switching functionalities of both of logic gates, confirming the viability of our TFTs for logic applications. Finally, combining all of these logic gates (NOR, NAND, and NOT gates), we have built a 2-bit half-adder circuit (Fig. 5 *A* and *B*). This circuit was designed to have two inputs (A and B) and two outputs (C, carry, and S, sum); C represents the 2^1 digit that yields a high output only when both inputs are high, whereas S represents the 2^0 digit that yields a high output only when either A or B input is high. To enable this circuit to function properly, 60 electrode pairs needed to be bridged. Fig. 5*C* is a zoomed-out image of our circuit substrate, whereas Fig. 5*D* are bright-field and cross-polarized optical images of a section of our circuit, demonstrating selective deposition and bridging of TIPS-pentacene crystals on the source/drain electrodes and within the channel region. Fig. 5*E* is the input–output characteristics of our circuit, which shows proper functionality as described above. Such a demonstration of a small-scale circuit using CONNECT opens up the possibility of building more complex system-level circuits over a large area in a facile manner.

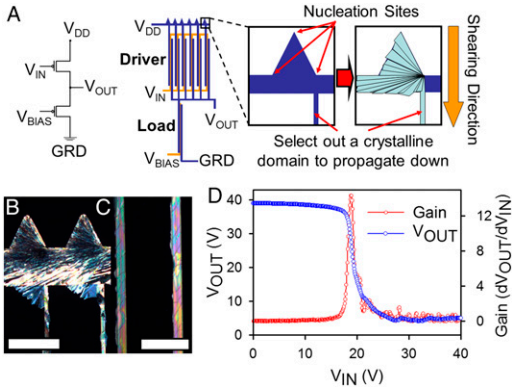

Fig. 4. Bridged OTFT-based PMOS inverter. (*A*) Circuit diagram and design layout of our PMOS inverter. The zoomed-in image depicts triangular design at the top used to induce nucleation and to subsequently select one crystalline domain to propagate down toward the electrodes. (*B*) Cross-polarized optical image of the triangular region showing nucleation and crystal growth. (Scale bar: 100 μm.) (*C*) Cross-polarized optical image showing a set of electrodes bridged with crystalline domains. (Scale bar: 100 μm.) (*D*) Representative voltage transfer curve with corresponding gain versus V_{IN} plot. Gain was 14.5.

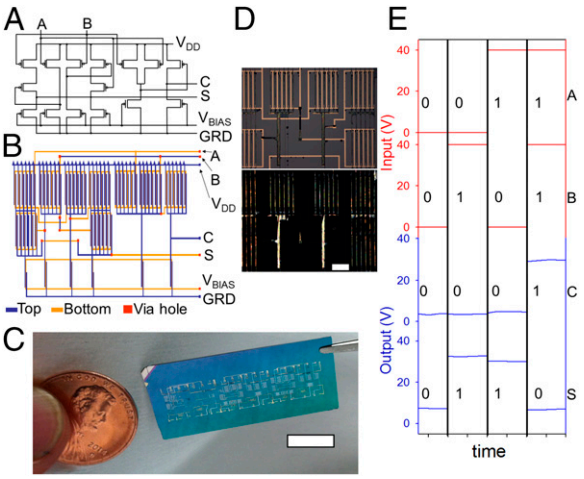

Fig. 5. Logic gates and 2-bit half-adder circuit. (*A*) Circuit diagram of 2-bit half-adder circuit. (*B*) Schematic layout of the 2-bit half-adder circuit design. Blue and yellow lines represent electrodes that are on the top and bottom of the dielectric layer, respectively, whereas red squares represent via holes. (*C*) Zoomed-out image of our circuit substrate. (Scale bar: 1 cm.) (*D*) Bright-field and crossed-polarized optical images of the 2-bit half-adder circuit, showing patterned and aligned TIPS-pentacene crystals on the top electrodes and within the channel regions. (Scale bar: 500 μm.) (*E*) Input–output voltage characteristics of our 2-bit half-adder circuit, showing proper logic functionality.

Bridging of Inkjet-Printed Patterns. To extend applicability of CONNECT to form low-cost, fully solution-processed organic electronics, inkjet-printed silver electrodes were used as bridging electrodes. Inkjet printing is a low-cost method of fabricating TFTs, but the channel spacing is limited to 15- to 20-μm resolution (57, 58). Fig. 6*A* and its *Inset* are crossed-polarized optical images of bridged inkjet-printed Ag electrodes, whereas Fig. 6*B* is transfer characteristics of several inkjet-printed TFTs. The highest mobility attained was 0.49 $cm^2/V{\cdot}s$ with an average of mobility of 0.24 $cm^2/V{\cdot}s$. The effectively bridged TFTs confirm that our technique not only works with lithographically patterned electrodes but also is transferrable to printed electrodes with larger channel lengths. This opens up a possibility of using our technique in conjunction with inkjet printing to yield perfectly aligned and patterned crystals between printed source and drain electrodes in a single step. Our technique is potentially advantageous over the inkjet printing of organic solutions as it is not limited by the printer's registration capacity and the size of the droplet. In addition, the crystalline domains can be aligned to yield more uniform device-to-device performance.

Discussion

Patterning, aligning, and controlling the charge transport of OSCs are paramount for creating large-area organic electronics. Various techniques have been developed to pattern OSCs such as templating, differential surface wetting, inkjet printing, and roll-to-roll printing (e.g., gravure, offset, flexographic printing) (3, 9, 13–15, 17, 25–29, 52). However, these techniques generally require extra steps to align the electrodes and the OSC layer, which can increase fabrication cost and reduce device yield. Inkjet printing (59–63) and roll-to-roll printing (27, 64–66) are the two most commonly used methods to fabricate organic circuits

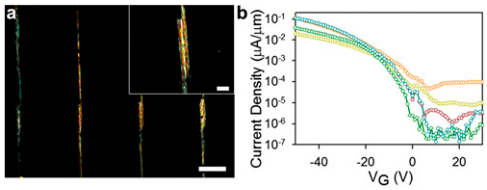

Fig. 6. Optical imaging of bridged TIPS-pentacene crystals on inkjet-printed silver electrodes. (*A*) Cross-polarized optical microscope image of the patterned TIPS-pentacene thin films on an array of silver electrodes. (Scale bar: 500 μm.) The *Inset* is a zoomed-in cross-polarized image of one of the TFTs showing TIPS-pentacene extending from one electrode to the other. (Scale bar: 100 μm.) (*B*) Transfer characteristics of several TFTs operated at $V_{DS} = -50$ V. The 300-nm SiO_2 and silicon substrate were used as dielectric layer and gate electrode, respectively.

and have the greatest potential for enabling large-area, low-cost organic electronics. These techniques, however, suffer from registration inaccuracies requiring large features and specially designed layouts and processes (27, 64, 66). The minimum feature sizes also vary widely, typically in the tens of micrometers range or higher (27, 67). These restrictions set a limit on the size and density of TFTs that can be achieved. Furthermore, inhomogeneity in film morphology and crystal orientation is also a significant issue at larger length scales (27, 66) that can lead to variability in electrical characteristics.

In the CONNECT process, we use the electrodes to define the solvent wetting regions. The OSCs only crystallize on the solvent wetting electrodes and across the channel, effectively creating self-patterned and precisely registered crystalline domains across the channel. Because registration and feature size are not limited by the capabilities of the instrument, our technique was able to achieve channel lengths and device-to-device pitch much smaller than many other solution-based printing techniques (27, 67). Furthermore, unlike many other solution-based deposition methods, our process is able to control the crystal orientation of the film during deposition, resulting in low variability in electrical properties. We were able to fabricated OTFT arrays with 99% yield, previously unseen in literature. We believe that our yield can be further improved by optimizing shearing conditions, for example by harnessing timescale of the diffusion lengths of the OSC in solution and matching it with the crystal growth rate. Using CONNECT, we created various logic gates and a 2-bit half-adder organic circuit to demonstrate that CONNECT is an industrially feasible method to fabricate large-area organic electronics. Finally, CONNECT was expanded to use with inkjet-printed silver electrodes, showing the versatility of this method to accommodate various solution deposition and fabrication methods of the rest of the components of the organic circuit. Our work represents a significant improvement in the formation of patterned OSCs and outlines a method of making complex organic circuits.

Materials and Methods

Materials. TIPS-pentacene, phenyl phosphonic acid, and thiophenol were purchased from Sigma-Aldrich, and OTS was purchased from Gelest. All chemicals were used as received (stored under an argon atmosphere to prevent hydrolysis). Silver nanoparticle ink for the inkjet-printed electrodes was purchased from Sigma-Aldrich. Highly doped *n*-type silicon wafers (resistivity, <0.005 Ω·cm) with a 300-nm thermally grown silicon oxide gate dielectric layer (capacitance of the gate dielectric per unit area, $C_{ox} = 10$ nF·cm^{-2}) were used as the substrates for OTFT fabrication.

Substrate Preparation and Characterization. The 300-nm-thick SiO_2 and silicon substrate were used as the dielectric layer and gate electrode, respectively. Electrodes were patterned using photolithography followed by the thermal evaporation of 2-nm Cr and 40-nm Au. The electrode width was set at 10 and 50 μm, whereas the channel length was set at 2 μm. The channel width was set at 500 or 1,000 μm. We note that side walls that are typically formed at the edge of the electrodes during the liftoff process resulted in poorly contacting TIPS-pentacene with the electrodes (i.e., voids were typically seen near the interface). This issue was circumvented by using a liftoff layer (LOL) to render the edge of the electrodes smooth (Fig. S10). LOL that was used was LOL2000, and it was spin cast on the SiO_2 surface at 3,000 rpm for 1 min. The LOL was then baked for 235 °C for 30 min. One micrometer of photoresist 3612 was then deposited on top of the LOL followed by 1-min bake at 90 °C. Exposure was conducted using ASML 5500 under 60 mJ/cm^2, followed by standard development procedure. Thereafter, 2 nm of Ti and 40 nm of Au were deposited, followed by liftoff in acetone; LOL was removed using Remover PG. The LOL is not a photosensitive material; however, it develops at a faster rate than photoresists. Hence, after development, the edges of the photoresist are lifted off of the substrate, allowing the subsequently deposited metal to be lifted off without side walls. The patterned substrate was treated with O_2 plasma at 200 mTorr and 150 W for 30 s. The substrate was then immersed in a 0.1% vol solution of OTS in trichloroethylene for 20 min, followed by rinsing with toluene and heating for 10 min on a hot plate at 120 °C. Thereafter, the substrate was immersed in 0.33% vol solution of thiophenol in ethanol for 10 s, followed by a toluene rinse. For inkjet printing, silicon oxide/silicon substrate was treated with UV ozone (UV/O_3) at 28 mW·cm^{-2} for 45 s to increase surface energy (from ∼44 to 70 mJ/mm^2) of the substrate, and thus to achieve well-defined electrode patterns. Ag ink was printed on the substrate with a piezoelectric inkjet printer (DMP-2831; Dimatix Corporation) and then sintered at 150 °C for 30 min in air. For narrow-channel formation, a 1-pL-volume ink cartridge that has 9-μm-diameter nozzles was used. The fabricated electrode width was about 30 μm; the channel width was 500 μm; and the channel length was about 15–20 μm. The OTS treatment was done on the inkjet-printed substrate using the same procedure stated above. The substrate was then immersed in 0.33% vol solution of phenyl phosphonic acid in ethanol for 10 s, followed by toluene rinse.

Solution Shearing of TIPS-Pentacene Films. The TIPS-pentacene solution was prepared at a concentration of 16 mg·mL^{-1} in toluene. Both the device substrate and the shearing plate were held in place by vacuum while the device substrate was mounted on a resistively heated stage (a thermoelectric module from Custom Thermoelectric) held at 80 °C. After placing ∼50 μL·cm^{-2} of TIPS-pentacene solution on the device substrate, the shearing plate was lowered with a micromanipulator to make contact with the solution. The device substrate was horizontal while the shearing plate was placed at a tilt angle of 1° from the horizontal. The gap distance between the device substrate and the shearing plate was fixed at 100 μm. The shearing plate was translated at different velocities by a stepper motor around 0.4 mm·s^{-1}. The resulting sheared film was left on the heating stage for 2–3 min at 90 °C to remove residual solvent. The meniscus contacts both the top and bottom substrate for the duration of our experiment; the solution does not dewet completely from either the shearing plate or the bottom substrate.

Solution-Sheared Film Characterizations. The solution-sheared films were characterized using a cross-polarized optical microscope (Leica DM4000M). Tapping-mode AFM was performed using a Multimode Nanoscope III (Digital Instruments/Veeco Metrology Group). Electrical measurements were conducted in a glove box under nitrogen using Keithley 4200 SC semiconductor analyzer.

Fabrication of Organic Circuit. Standard photolithography was used to pattern the bottom-gate bottom-contact logic gates and circuits. The gate and the source drain electrodes were composed of 2 nm of Cr and 40 nm of Au. The 300 nm of silicon oxide was deposited on gate electrode using low-pressure chemical vapor deposition. Via holes were made using wet-chemical HF etching.

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